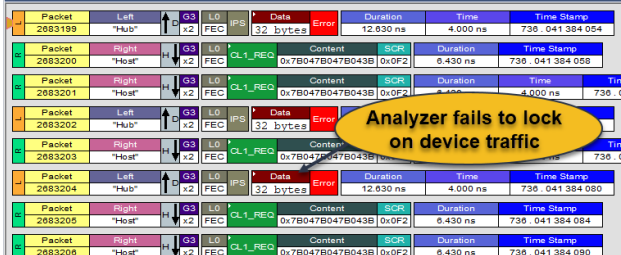


USB4 Low Power Exit Issue

Overview: The Microsoft Windows® 11 Connection Manager utilizes aggressive power management on USB4 links. Some Voyager M4x users testing with Windows 11 may experience issues consistently re-locking after low power exit. This issue affects the Voyager M4x in USB4 “Analyzer Mode” where one or both transceivers may occasionally fail to lock on incoming data. If one side fails to lock, the trace will be full of IPS events. If both fail to lock, no valid traffic will appear in the trace.



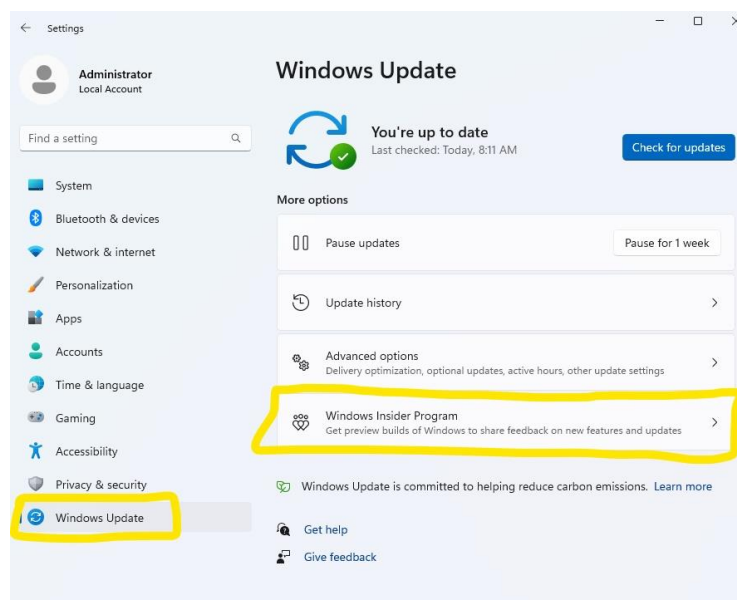
Packet	Left	Right	Q3	Q2	Q1	Q0	IPS	Data	Error	Duration	Time	Time Stamp
2683199	Hub	Hub	Q3	Q2	Q1	Q0	FEC	32 bytes	Error	12.830 ns	4.000 ns	736.041384054
2683200	Host	Host	Q3	Q2	Q1	Q0	FEC	Content	SCR	6.430 ns	736.041384058	
2683201	Host	Host	Q3	Q2	Q1	Q0	CL1_REQ	Content	SCR	4.000 ns	736.041384062	
2683202	Hub	Hub	Q3	Q2	Q1	Q0	FEC	32 bytes	Error	12.830 ns	4.000 ns	736.041384066
2683203	Host	Host	Q3	Q2	Q1	Q0	FEC	Content	SCR	6.430 ns	736.041384070	
2683204	Hub	Hub	Q3	Q2	Q1	Q0	FEC	32 bytes	Error	12.830 ns	4.000 ns	736.041384074
2683205	Host	Host	Q3	Q2	Q1	Q0	FEC	Content	SCR	6.430 ns	736.041384078	
2683206	Host	Host	Q3	Q2	Q1	Q0	CL1_REQ	Content	SCR	4.000 ns	736.041384082	

“IPS” or “garbage” packets from one or both sides may indicate analyzer failed to lock after low power exit

After months of sustained effort to improve the lock performance, the issue appears to be a limitation within the FPGA transceivers. In many cases, real USB4 chipsets may lock before the analyzer can recover the clock resulting in IPS events or “garbage traffic”. While efforts to improve this issue will continue at Teledyne LeCroy, the only consistent work-around at this time is to disable low power entry on the system-under-test.

Workaround: Microsoft Windows 11 has recently added registry control for disabling entry to low power states (CLx) on the USB4 logical link (beginning with rs_prerelease 25192.1000). Use the following steps to disable CLx for Windows 11 environments.

1. Enroll in Windows Insider Dev Channel: <https://insider.windows.com/en-us/for-developers-getting-started>



2. Install latest Dev Channel build (25192.1000 or later)

Test Mode
Windows 11 Pro Insider Preview
Evaluation copy. Build 25197.rs_prerelease.220902-1559

3. Enable test signing via Command Prompt (*bcdedit /set testsigning on*)

*NOTE: Test Signing must be enabled through an Administrator Account

```
C:\> Select Administrator: Command Prompt

Microsoft Windows [Version 10.0.25197.1000]
(c) Microsoft Corporation. All rights reserved.

C:\Users\Administrator>bcdedit /set testsigning on
The operation completed successfully.

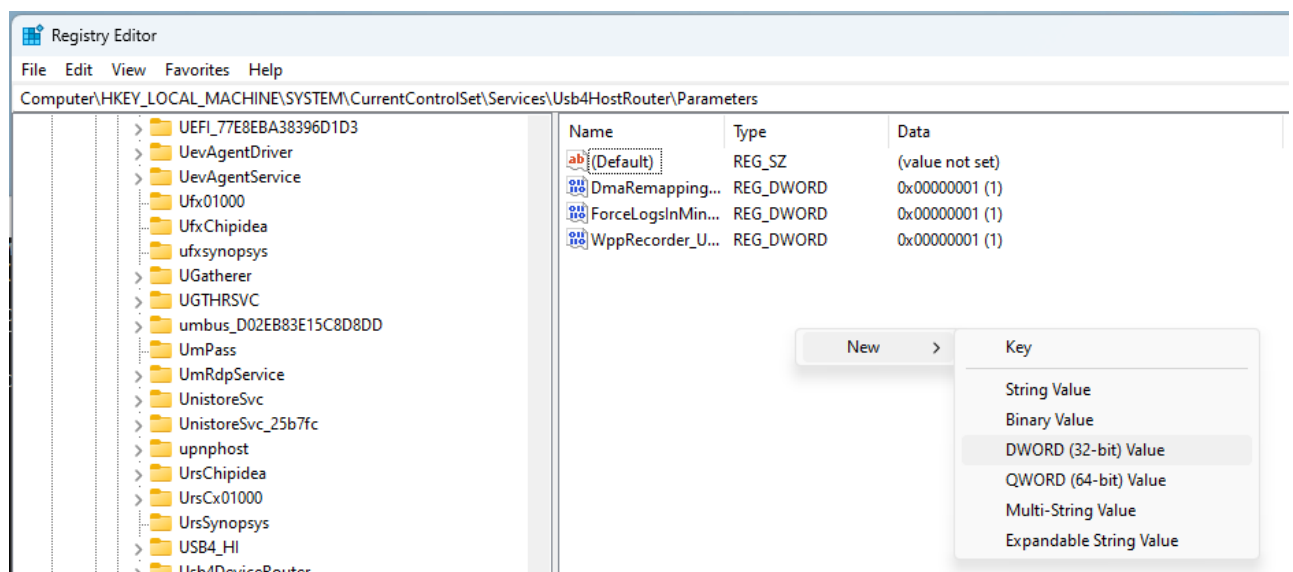
C:\Users\Administrator>
```

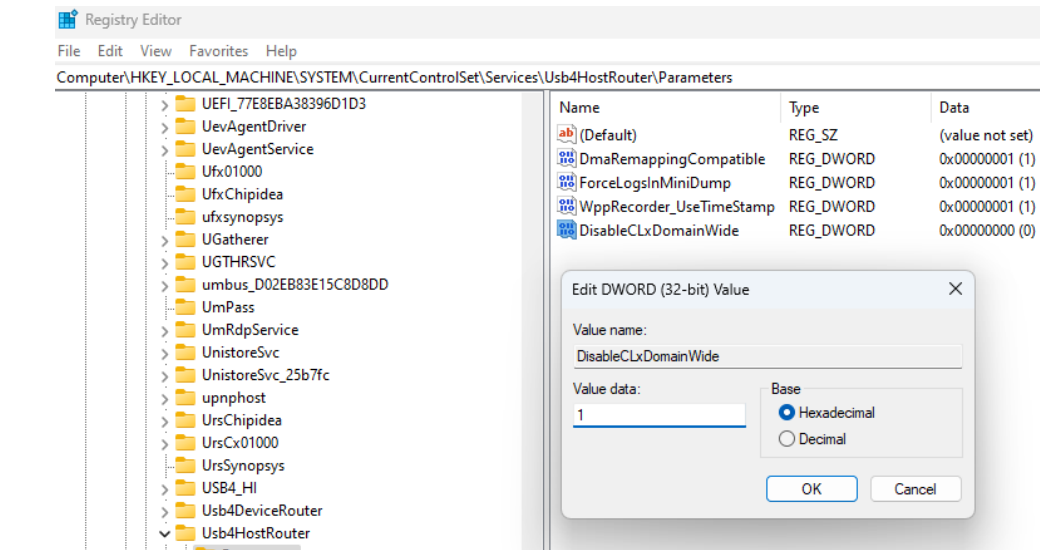
4. Set the following registry key:

HKLM\ SYSTEM\CurrentControlSet\Services\Usb4HostRouter\Parameters

Create DWORD "DisableCLxDomainWide"

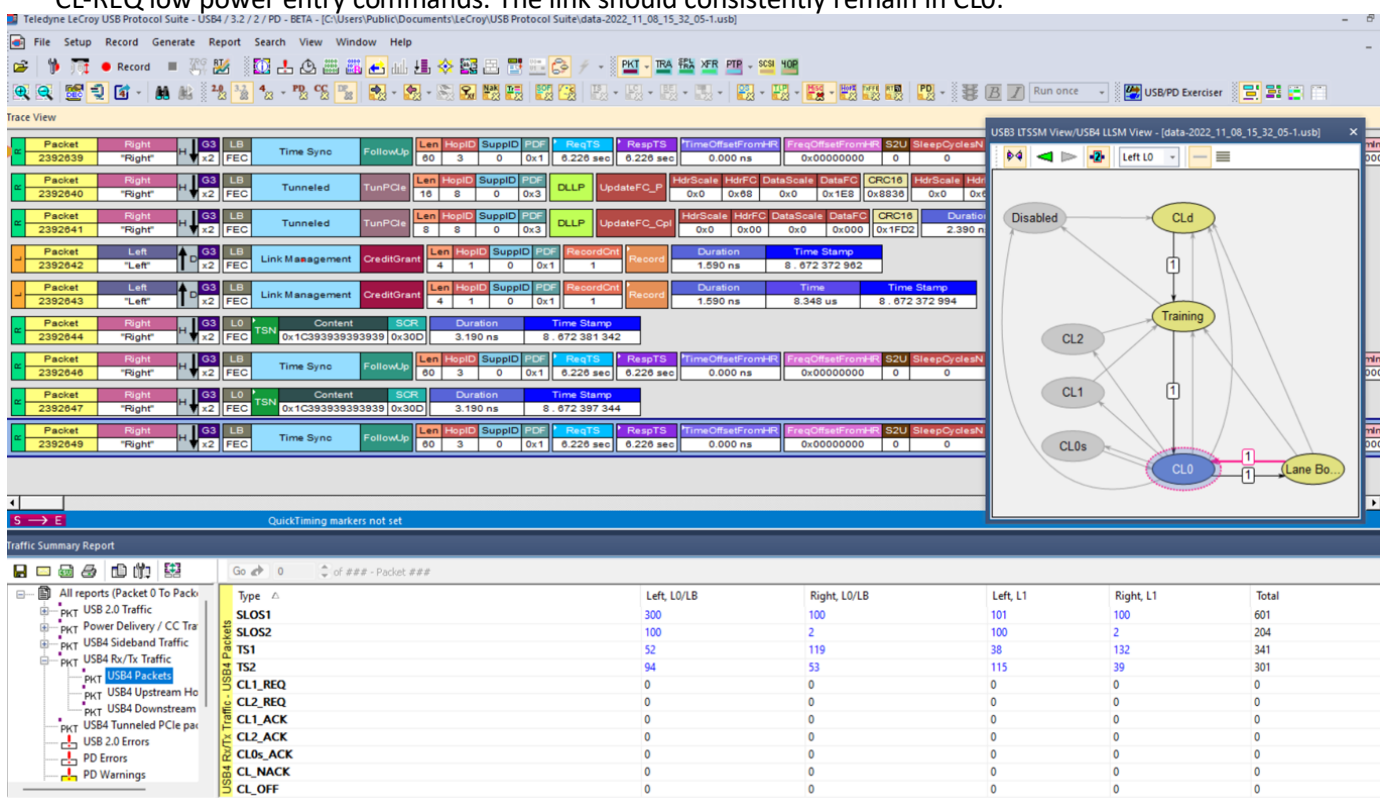
Set to 1 to disable CLx. (Set to 0 or delete the key to disengage the test hook)





5. Reboot to enact this change in settings.

6. After reboot, the trace captures should indicate that Windows Connection Manager is no longer issuing CL-REQ low power entry commands. The link should consistently remain in CL0.



Packet	Direction	Protocol	Length	Host ID	Supp ID	Port	Req TS	Resp TS	Time Offset From #1	Freq Offset From #1	S2U	Sleep Cycle
2392639	Right	FE	10	3	0	0x1	6.226 sec	6.226 sec	0.000 ns	0x00000000	0	0
2392640	Right	FE	10	8	0	0x3	6.226 sec	6.226 sec	0.000 ns	0x00000000	0	0
2392641	Right	FE	10	8	0	0x3	6.226 sec	6.226 sec	0.000 ns	0x00000000	0	0
2392642	Left	FE	4	1	0	0x1	1.590 ns	8.672 372 992	1.590 ns	8.348 us	8.672 372 994	
2392643	Left	FE	4	1	0	0x1	1.590 ns	8.672 372 992	1.590 ns	8.348 us	8.672 372 994	
2392644	Right	FE	10	3	0	0x1	6.226 sec	6.226 sec	0.000 ns	0x00000000	0	0
2392646	Right	FE	10	8	0	0x3	6.226 sec	6.226 sec	0.000 ns	0x00000000	0	0
2392647	Right	FE	10	8	0	0x3	6.226 sec	6.226 sec	0.000 ns	0x00000000	0	0
2392649	Right	FE	10	3	0	0x1	6.226 sec	6.226 sec	0.000 ns	0x00000000	0	0

Type	Left, L0/LB	Right, L0/LB	Left, L1	Right, L1	Total
SLOS1	300	100	101	100	601
SLOS2	100	2	100	2	204
TS1	52	119	38	132	341
TS2	94	53	115	39	301
CL1_REQ	0	0	0	0	0
CL2_REQ	0	0	0	0	0
CL1_ACK	0	0	0	0	0
CL2_ACK	0	0	0	0	0
CL0s_ACK	0	0	0	0	0
CL_NACK	0	0	0	0	0
CL_OFF	0	0	0	0	0